WHAT IS CLAIMED IS:

1. A method comprising:

writing a first set of data into a first memory element during a first time interval;

writing a second set of data into a second memory element during a second time interval;

reading a portion of the first set of data from the first memory element during the second time interval;

reading a portion of the second set of data from the second memory element during a third time interval; and

determining the first, second, and third time intervals based on a format of the sets of data, with the first time interval ending before the second time interval begins, and the second time interval ending before the third time interval begins.

2. The method of claim 1 wherein the first set of data and the second set of data each comprise a portion of an incoming data stream.

3. The method of claim 2 further comprising:

determining the portion of the first set of data based on connection information associated with the incoming data stream; and

determining the portion of the second set of data based on the connection information.

4. The method of claim 1 wherein writing the first set of data is performed over a bi-directional port, and reading a portion of the first set of data is performed over the bi-directional port.

5. The method of claim 1 wherein writing the second set of data is performed over a bi-directional port, and reading a portion of the second set of data is performed over the bi-directional port.

6. The method of claim 1 wherein writing the first set of data is performed over a plurality of bi-directional ports, and reading a portion of the first set of data is performed over the plurality of bi-directional ports.

7. The method of claim 1 wherein writing the second set of data is performed over a plurality of bi-directional ports, and reading a portion of the second set of data is performed over the plurality of bi-directional ports.

8. The method of claim 1 wherein the determining occurs prior to writing the first and second sets of data and reading the portions of the first and second sets of data.

9. The method of claim 1 wherein the first set of data and the second set of data each comprise a portion of a block of data having one of a plurality of types of low-order multiplexing formats.

10. The method of claim 9 wherein the determining comprises:

determining a size of memory space used to store the first set of data within the first memory element, and determining time used to access the determined size of memory space used to store the first set of data; and

determining a size of memory space used to store the second set of data within the second memory element, and determining time used to access the determined size of memory space used to store the second set of data.

11. The method of claim 10 wherein the size of memory space used to store the first set of data and the size of memory space used to store the second set of data are based on the plurality of types of low-order multiplexing formats.

12. An apparatus comprising:

an input write bus;

a first memory element in electrical communication with the input write bus;

a second memory element in electrical communication with the input write bus; and

circuitry configured to

write a first set of data into the first memory element during a first time interval;

write a second set of data into the second memory element during a second time interval;

read a portion of the first set of data from the first memory element during the second time interval;

read a portion of the second set of data from the second memory element during a third time interval; and

determine the first, second, and third time intervals based on a format of the sets of data, with the first time interval ending before the second time interval begins, and the second time interval ending before the third time interval begins.

13. The apparatus of claim 12 wherein the first set of data and the second set of data each comprise a portion of an incoming data stream applied to the write bus.

14. The apparatus of claim 13 further comprising:

a third memory element in electrical communication with the input write bus;

a fourth memory element in electrical communication with the input write bus; and

a fifth memory element in electrical communication with the input write bus.

15. The apparatus of claim 14 wherein the circuitry is further configured to store portions of the incoming data stream in each of the third, fourth, and fifth memory elements.

16. The apparatus of claim 13 further comprising a connection memory configured to store connection information associated with the incoming data stream.

17. The apparatus of claim 16 further comprising a read address generator configured to:

determine the portion of the first set of data based on the connection information; and

determine the portion of the second set of data based on the connection information.

18. A computer program product tangibly embodied on a computer readable medium, for provisioning cross-connects in network switching environment comprising instructions for causing a computer to:

write a first set of data into a first memory element during a first time interval;

write a second set of data into a second memory element during a second time interval;

read a portion of the first set of data from the first memory element during the second time interval;

read a portion of the second set of data from the second memory element during a third time interval; and

determine the first, second, and third time intervals based on a format of the sets of data, with the first time interval ending before the second time interval begins, and the second time interval ending before the third time interval begins.